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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	P3817
First Inventor	Mario Nemirovsky et al.
Title	Clustering Stream and/or Instruction Queues for Multi-Streaming Processors
Express Mail Label No.	EL573446755US

JC960 U.S. PTO 09/706157 11/03/00

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

1. [X] Fee Transmittal Form (e.g., PTO/SB/17) *(Submit an original and a duplicate for fee processing)*
2. [X] Applicant claims small entity status. See 37 CFR 1.27.
3. [X] Specification [Total Pages 14] *(preferred arrangement set forth below)*
   - Descriptive title of the invention
   - Cross Reference to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to sequence listing, a table, or a computer program listing appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings (*if filed*)
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
4. [X] Drawing(s) *(35 U.S.C. 113)* [Total Sheets 4]
5. Oath or Declaration [Total Pages 2]
   a. [X] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 CFR 1.63 (d)) *(for continuation/divisional with Box 17 completed)*
      i [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b)
6. [ ] Application Data Sheet. See 37 CFR 1.76
7. [ ] CD-ROM or CD-R in duplicate, large table or Computer Program (*Appendix*)
8. Nucleotide and/or Amino Acid Sequence Submission (*if applicable, all necessary*)
   a. [ ] Computer Readable Form (CRF)
   b. Specification Sequence Listing on:
      i. [ ] CD-ROM or CD-R (2 copies); or
      ii. [ ] paper
   c. [ ] Statements verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

9. [X] Assignment Papers (cover sheet & document(s))
10. [ ] 37 CFR 3.73(b) Statement *(when there is an assignee)* [X] Power of Attorney
11. [ ] English Translation Document *(if applicable)*
12. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
13. [ ] Preliminary Amendment
14. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
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[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No. _____/_____

Prior application information Examiner NA Group / Art Unit NA

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Name (Print/Type)	Donald R. Boys	Registration No. (Attorney/Agent)	35,074
Signature		Date	11/03/2000

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FEE TRANSMITTAL for FY 2001

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TOTAL AMOUNT OF PAYMENT ($) 395.00

Complete if Known	
Application Number	NA
Filing Date	11/03/2000
First Named Inventor	Mario Nemirovsky et al.
Examiner Name	NA
Group Art Unit	NA
Attorney Docket No.	P3817

METHOD OF PAYMENT

1. [X] The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to:
   Deposit Account Number: 500534
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   [X] Applicant claims small entity status See 37 CFR 1.27
2. [X] **Payment Enclosed:** [X] Check [ ] Credit card [ ] Money Order [ ] Other

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1. BASIC FILING FEE

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101	710	201	355	Utility filing fee	355.00
106	320	206	160	Design filing fee	
107	490	207	245	Plant filing fee	
108	710	208	355	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 355.00

2. EXTRA CLAIM FEES

	Extra Claims		Fee from below	Fee Paid
Total Claims	16 - 20** = 0	X	9	= 0.00
Independent Claims	2 - 3** = 0	X	40	= 0.00
Multiple Dependent				= 0.00

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	80	202	40	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim, if not paid
109	80	209	40	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

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FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for *ex parte* reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	390	216	195	Extension for reply within second month	
117	890	217	445	Extension for reply within third month	
118	1,390	218	695	Extension for reply within fourth month	
128	1,890	228	945	Extension for reply within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,240	241	620	Petition to revive - unintentional	
142	1,240	242	620	Utility issue fee (or reissue)	
143	440	243	220	Design issue fee	
144	600	244	300	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	40
146	710	246	355	Filing a submission after final rejection (37 CFR § 1.129(a))	
149	710	249	355	For each additional invention to be examined (37 CFR § 1.129(b))	
179	710	279	355	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	
Other fee (specify)					

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 40.00

SUBMITTED BY				Complete (if applicable)	
Name (Print/Type)	Donald R. Boys	Registration No. (Attorney/Agent)	35,074	Telephone	(831) 726-1457
Signature				Date	11/03/2000

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VERIFIED STATEMENT CLAIMING SMALL ENTITY STATUS (37 CFR 1.9(f) & 1.27(c))--SMALL BUSINESS CONCERN	Docket Number (Optional) P3817

Applicant or Patentee: Mario Nemirovsky et al.
Application or Patent No.: NA
Filed or Issued: NA
Title: Clustering Stream and/or Instruction Queues for Multi-Streaming Processors

I hereby declare that I am
☐ the owner of the small business concern identified below:
☑ an official of the small business concern empowered to act on behalf of the concern identified below:

NAME OF SMALL BUSINESS CONCERN XStream Logic, Inc.

ADDRESS OF SMALL BUSINESS CONCERN 750 University Ave. St. 270
Los Gatos, CA 95032

I hereby declare that the above identified small business concern qualifies as a small business concern as defined in 13 CFR 121.12, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees to the United States Patent and Trademark Office, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time, or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

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☑ the specification filed herewith with title as listed above.
☐ the application identified above.
☐ the patent identified above.

If the rights held by the above identified small business concern are not exclusive, each individual, concern, or organization having rights in the invention must file separate verified statements averring to their status as small entities, and no rights to the invention are held by any person, other than the inventor, who would not qualify as an independent inventor under 37 CFR 1.9(c) if that person made the invention, or by any concern which would not qualify as a small business concern under 37 CFR 1.9(d), or a nonprofit organization under 37 CFR 1.9(e).

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NAME OF PERSON SIGNING Dan O'Neill

TITLE OF PERSON IF OTHER THAN OWNER President and CEO

ADDRESS OF PERSON SIGNING 750 University Ave., Los Gatos, CA 95032

SIGNATURE Dan O'Neill DATE Nov 1 2000

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Clustering Stream and/or Instruction Queues for Multi-Streaming Processors

by inventors
Mario Nemirovsky, Stephen W. Melvin and Nandakumar Sampath, Enric Musoll, and Hector Urdaneta

Field of the Invention

The present invention is in the field of digital processing and pertains more particularly to architecture and operation in dynamic multistreaming processors.

Background of the Invention

Conventional pipelined single-stream processors incorporate fetch and dispatch pipeline stages, as is true of most conventional processors. In such processors, in the fetch stage, one or more instructions are read from an instruction cache and in the dispatch stage, one or more instructions are sent to execution units (EUs) to execute. The stages may be separated by one or more other stages, for example a decode stage. In such a processor the fetch and dispatch stages are coupled together such that the fetch stage generally fetches from the instruction stream in every cycle.

In multistreaming processors known to the present inventors, multiple instruction streams are provided, each having access to the execution units. Multiple fetch stages may be provided, one for each instruction stream, although one dispatch stage is employed. Thus, the fetch and dispatch stages are coupled to one another as in other conventional processors, and each instruction stream generally fetches instructions in each cycle. That is, if there are five instruction streams, each of the five fetches in

each cycle, and there needs to be a port to the instruction cache for each stream, or a separate cache for each stream.

In a multistreaming processor multiple instruction streams share a common set of resources, for example execution units and/or access to memory resources. In such a processor, for example, there may be M instruction streams that share Q execution units in any given cycle. This means that a set of up to Q instructions is chosen from the M instruction streams to be delivered to the execution units in each cycle. In the following cycle a different set of up to Q instructions is chosen, and so forth. More than one instruction may be chosen from the same instruction stream, up to a maximum P, given that there are no dependencies between the instructions.

It is desirable in multistreaming processors to maximize the number of instructions executed in each cycle. This means that the set of up to Q instructions that is chosen in each cycle should be as close to Q as possible. Reasons that there may not be Q instructions available include flow dependencies, stalls due to memory operations, stalls due to branches, and instruction fetch latency.

A further difficulty in multi-streaming processors, particularly is such processors having a relatively large number of streams, is in operating the processor over all of the streams.

What is clearly needed in the art is an apparatus and method to cluster streams in a multi-streaming processor, such that separate clusters can operate substantially independently. The present invention, in several embodiments described in enabling detail below, provides a unique solution.

Summary of the Invention

In a preferred embodiment of the present invention a pipelined multistreaming processor is provided, comprising an instruction source, a first cluster of a plurality of streams fetching instructions from the instruction source, a second cluster of a plurality of streams fetching instructions from the instruction source, dedicated instruction queues for individual streams in each cluster, a first dedicated dispatch stage in the first cluster for dispatching instructions to execution units, and a second dedicated dispatch stage in the second cluster for selecting and dispatching instructions to execution units. The processor is characterized in that the clusters operate independently, with the dedicated dispatch stage taking instructions only from the instruction queues in the individual clusters to which the dispatch stages are dedicated.

In some embodiments individual ones or groups of execution units are associated with and dedicated for use by individual clusters. Also in some embodiments individual streams in a cluster have one or both of dedicated fetch and dispatch stages. In a particular embodiment the total number of streams in the processor is eight, with four streams in each cluster, and one stream from each cluster fetches instructions from the instruction source in each cycle. Further, in the particular embodiment, the select system may monitor a set of fetch program counters (FPC) having one FPC dedicated to each stream, and direct fetching if instructions beginning at addresses according to the to the program counters. Still further, in a particular embodiment, each stream selected to fetch for a cluster is directed to fetch eight instructions from the instruction source.

In some cases there may be one or more general execution units to which either or both dispatch stages may dispatch instructions. Also in preferred embodiments, each stream in each cluster has an associated instruction queue.

In another aspect of the invention, in a pipelined multistreaming processor having an instruction source and a plurality of streams, a method for simplifying implementation and operation of the streams is provided, comprising the steps of (a) clustering the streams into two or more clusters, with each cluster having a fetch stage; (b) dedicating a dispatch stage to each cluster, for dispatching instructions to execution units; and (c) fetching, in each cycle, a series of instructions from the instruction source by a single cluster.

In some embodiments of this method there groups of execution units dedicated to each cluster, to which the dispatch stages in that cluster may dispatch instructions. There are also, in some embodiments, one or both of fetch or dispatch stages dedicated to individual streams in a cluster. In a particular embodiment the total number of streams in the processor is eight, and the number of streams in each cluster is four. Also in a particular embodiment the select system monitors a set of fetch program counters (FPC) having one FPC associated with each stream, and directs fetching of instructions beginning at addresses according to the program counters. Further in a particular embodiment each stream selected to fetch is directed to fetch eight instructions from the instruction source.

In some embodiments of the method the processor further comprises one or more general execution units, and each dispatch stage is enabled to dispatch instructions to the general execution units. Also in some embodiments each stream in each cluster has an instruction queue associated with that stream, and further comprising a step for dispatching instructions

to execution units dedicated to each cluster from the instruction queues associated with the streams in each cluster.

In embodiments of the present invention, described in enabling detail below, for the first time a pipelined, multi-streaming processor is provided, wherein streams may be clustered, and operations may therefore be more efficiently accomplished.

Brief Description of the Drawings

Fig. 1 is a block diagram depicting a pipelined structure for a processor in the prior art.

Fig. 2 is a block diagram depicting a pipelined structure for a multistreaming processor known to the present inventors.

Fig. 3 is a block diagram for a pipelined architecture for a multistreaming processor according to an embodiment of the present invention.

Fig. 4 is a block diagram for a pipelined architecture for a multistreaming processor according to another embodiment of the present invention.

Description of the Preferred Embodiments

Fig. 1 is a block diagram depicting a pipelined structure for a processor in the prior art. In this prior art structure there is an instruction cache 11, wherein instructions await selection for execution, a fetch stage 13 which selects and fetches instruction into the pipeline, and a dispatch stage

which dispatches instructions to execution units (EUs) 17. In many conventional pipelined structures there are additional stages other than the exemplary stages illustrated here.

In the simple architecture illustrated in Fig. 1 everything works in lockstep. In each cycle an instruction is fetched, and another previously fetched instruction is dispatched to one of the execution units.

Fig. 2 is a block diagram depicting a pipelined structure for a multistreaming processor known to the present inventors, wherein a single instruction cache 19 has ports for three separate streams, and one instruction is fetched per cycle by each of three fetch stages 21, 23 and 25 (one for each stream). In this particular case a single dispatch stage 27 selects instructions from a pool fed by the three streams and dispatches those instructions to one or another of three execution units 29. In this architecture the fetch and dispatch units are still directly coupled. It should be noted that the architecture of Fig. 2, while prior to the present invention, is not necessarily in the public domain, as it is an as-yet proprietary architecture known to the present inventors. In another example, there may be separate caches for separate streams, but this does not provide the desired de-coupling.

Fig. 3 is a block diagram depicting an architecture for a dynamic multistreaming (DMS) processor according to an embodiment of the present invention. In this DMS processor there are eight streams and ten functional units, which may also be called execution units. Instruction cache 31 in this embodiment has two ports for providing instructions to fetch stage 33. Eight instructions may be fetched each cycle for each port, so 16 instructions may be fetched per cycle. The fetch stage is not explicitly shown in the staged pipeline as per the previous examples, but is described further below.

In a preferred embodiment of the present invention instruction queues 39 are provided, which effectively the couple fetch and dispatch

stages in the pipeline. There are in this embodiment eight instruction queues, one for each stream. In the example of Fig. 3 the instruction queues are shown in a manner to illustrate that each queue may have a different number of instructions ready for transfer to a dispatch stage 41.

Referring again to instruction cache 31 and the two ports to fetch stage 33, it was described above that eight instructions may be fetched to fetch stage 33 by each port. Typically the eight instructions for one port are eight instructions from a single thread for a single stream. For example, the eight instructions fetched by one port in a particular cycle will typically be sequential instructions for a thread associated with one stream.

Determination of the two threads associated with two streams to be accessed in each cycle is made by selection logic 35. Logic 35 monitors a set of fetch program counters 37, which maintain a program counter for each stream, indicating at what address to find the next instruction for that stream. Select logic 35 also monitors the state of each queue in set 39 of instruction queues. Based at least in part on the state of instruction queues 39 select logic 35 determines the two threads from which to fetch instructions in a particular cycle. For example, if the instruction queue in set 39 for a stream is full, the probability of utilizing eight additional instructions into the pipeline from the thread associated with that stream is low. Conversely, if the instruction queue in set 39 for a stream is empty, the probability of utilizing eight additional instructions into the pipeline from the thread associated with that stream is high.

In this embodiment, in each cycle, four instructions are made available to dispatch stage 41 from each instruction queue. In practice dispatch logic is provided for selecting from which queues to dispatch instructions. The dispatch logic has knowledge of many parameters,

typically including priorities, instruction dependencies, and the like, and is also aware of the number of instructions in each queue.

As described above, there are in this preferred embodiment ten execution units, which include two memory units 43 and eight arithmetic logic units (ALUs) 45. Thus, in each cycle up to ten instructions may be dispatched to execution units.

In the system depicted by Fig. 3 the unique and novel set of instruction queues 39 provides decoupling of dispatch from fetch in the pipeline. The dispatch stage now has a larger pool of instructions from which to select to dispatch to execution units, and the efficiency of dispatch is improved. That is the number of instructions that may be dispatched per cycle is maximized. This structure and operation allows a large number of streams of a DMS processor to execute instructions continually while permitting the fetch mechanism to fetch from a smaller number of streams in each cycle. Fetching from a smaller number of streams, in this case two, in each cycle is important, because the hardware and logic necessary to provide additional ports into the instruction cache is significant. As an added benefit, unified access to a single cache is provided.

Thus the instruction queue in the preferred embodiment allows fetched instructions to be buffered after fetch and before dispatch. The instruction queue read mechanism allows the head of the queue to be presented to dispatch in each cycle, allowing a variable number of instructions to be dispatched from each stream in each cycle. With the instruction queue, one can take advantage of instruction stream locality, while maximizing the efficiency of the fetch mechanism in the presence of stalls and branches. By providing a fetch mechanism that can support up to eight instructions from two streams, one can keep the instruction queues full while not having to replicate the fetch bandwidth across all streams.

Clustering Streams and/or Instruction Queues

In an alternative embodiment of the present invention a further innovation is made in a multistreaming processor which may or may not have instruction queues associated with streams

Fig. 4 is a block diagram for a pipelined architecture for a multistreaming processor according to another embodiment of the present invention. In the processor illustrated by Fig. 4 there are eight streams, just as in the processor of Fig. 3. There are also eight fetch stages, one for each stream, and a full set of execution units. In this example there are instruction queues shown, one for each stream, but the presence of these queues is not required for the present invention. A salient difference from architecture previously described is that the plurality of streams is grouped into two distinct clusters.

Referring again to Fig. 4, instructions are fetched from instruction cache 47 by two stream clusters 49 and 51, labeled Cluster A and Cluster B. Cluster A comprises four streams, each having a fetch stage 63 and a set of instruction queues 65, one for each stream. The instruction queues operate as described above for the processor of Fig. 3. Cluster A further has a dispatch stage 67 for the four streams in the cluster, which dispatches instructions from queues 65 to a set of functional, or execution units 69.

Cluster B (51) has the same structure as Cluster A, comprising four streams, each with a fetch stage in set 55, each having an instruction queue in set 57, and a dedicated dispatch stage 59 which dispatches instructions from the instruction queues to a set of execution (functional) units 61.

In some embodiments of this unique architecture there are one or more general execution units (GXU) 71, to which instructions may be dispatched

by either of dispatch stages 67 or 59. The clusters share a common data cache 53.

Instruction cache 47 still has two ports, as in the previously described embodiment, and there is a select system, much as previously described, for selecting which stream in each cycle in each Cluster will fetch instructions. The select system has access, as before, to FPCs, and monitors the state of each instruction queue in each Cluster. In the present case one stream of four in each Cluster is selected each cycle to fetch eight sequential instructions beginning at the PC address.

Referring again to Fig. 4, there are two dispatch stages, one for each cluster, each of which dispatches instructions from only the queues in its own associated Cluster.

A distinct advantage in clustering streams with use of instruction queues as described and taught herein, is that the overall complexity, hence cost, of implementing two 4x4 clusters is less than implementing the 8x8 array described with the aid of Fig. 3.

The skilled artisan will recognize that there are a number of alterations that might be made in embodiments of the invention described above without departing from the spirit and scope of the invention. For example, the number of instruction queues may vary, the number of ports into the instruction cache may vary, the fetch logic may be implemented in a variety of ways, and the dispatch logic may be implemented in a variety of ways, among other changes that may be made within the spirit and scope of the invention. There also be a different Clustering of streams than that depicted and described as an example herein. For these and other reasons the invention should be afforded the broadest scope, and should be limited only by the claims that follow.

What is claimed is:

1. A pipelined multistreaming processor, comprising:

an instruction source;

a first cluster of a plurality of streams fetching instructions from the instruction source;

a second cluster of a plurality of streams fetching instructions from the instruction source;

dedicated instruction queues for individual streams in each cluster;

a first dedicated dispatch stage in the first cluster for dispatching instructions to execution units; and

a second dedicated dispatch stage in the second cluster for dispatching instructions to execution units;

characterized in that the clusters operate independently, with the dedicated dispatch stage taking instructions only from the instruction queues in the individual clusters to which the dispatch stages are dedicated.

2. The processor of claim 1 wherein individual ones or groups of execution units are associated with and dedicated for use by individual clusters.

3. The processor of claim 1 wherein individual streams in a cluster have dedicated fetch stages.

4. The processor of claim 1 wherein the total number of streams in the processor is eight, with four streams in each cluster.

5. The processor of claim 1 wherein instructions are fetched in each cycle for one stream in each cluster.

6. The processor of claim 1 wherein the a set of fetch program counters (FPC) are monitored with one FPC dedicated to each stream, and fetching of instructions is directed beginning at addresses according to the program counters.

7 The processor of claim 4 wherein eight instructions are fetched for a stream each time instructions are fetched for that stream.

8. The processor of claim 2 further comprising one or more execution units to which either or both dispatch stages may dispatch instructions.

9. In a pipelined multistreaming processor having an instruction source and a plurality of streams, a method for simplifying implementation and operation of the streams, comprising the steps of:

(a) clustering the streams into two or more clusters;

(b) dedicating a single dispatch stage to each cluster, for dispatching instructions to execution units; and

(c) fetching, in each cycle, a series of instructions from the instruction source by a single cluster.

10. The method of claim 9 further comprising groups of execution units dedicated to each cluster, to which the dispatch stages in that cluster may dispatch instructions.

11. The method of claim 9 further comprising fetch stages dedicated to individual streams in a cluster.

12. The method of claim 9 wherein the total number of streams in the processor is eight, and the number of streams in each cluster is four.

13. The method of claim 9 having a fetch program counter (FPC) associated with each stream, wherein fetching is directed beginning at addresses according to the program counters.

14. The method of claim 9 wherein eight instructions are fetched each time instructions are fetched for a stream

15. The method of claim 9 wherein the processor further comprises one or more general execution units, and each dispatch stage is enabled to dispatch instructions to the general execution units.

16. The method of claim 9 wherein each stream in each cluster has an instruction queue associated with that stream, and further comprising a step for dispatching instructions to execution units dedicated to each cluster from the instruction queues associated with the streams in each cluster.

Abstract of the Disclosure

A pipelined multistreaming processor has an instruction source, a first cluster of a plurality of streams fetching instructions from the instruction source, a second cluster of a plurality of streams fetching instructions from the instruction source, dedicated instruction queues for individual streams in each cluster, a first dedicated dispatch stage in the first cluster for dispatching instructions to execution units, and a second dedicated dispatch stage in the second cluster for selecting and dispatching instructions to execution units. The processor is characterized in that the clusters operate independently, with the dedicated dispatch stage taking instructions only from the instruction queues in the individual clusters to which the dispatch stages are dedicated. In preferred embodiments there are dedicated fetch and dispatch stages for streams in the clusters, and dedicated execution units to which instructions may be dispatched.

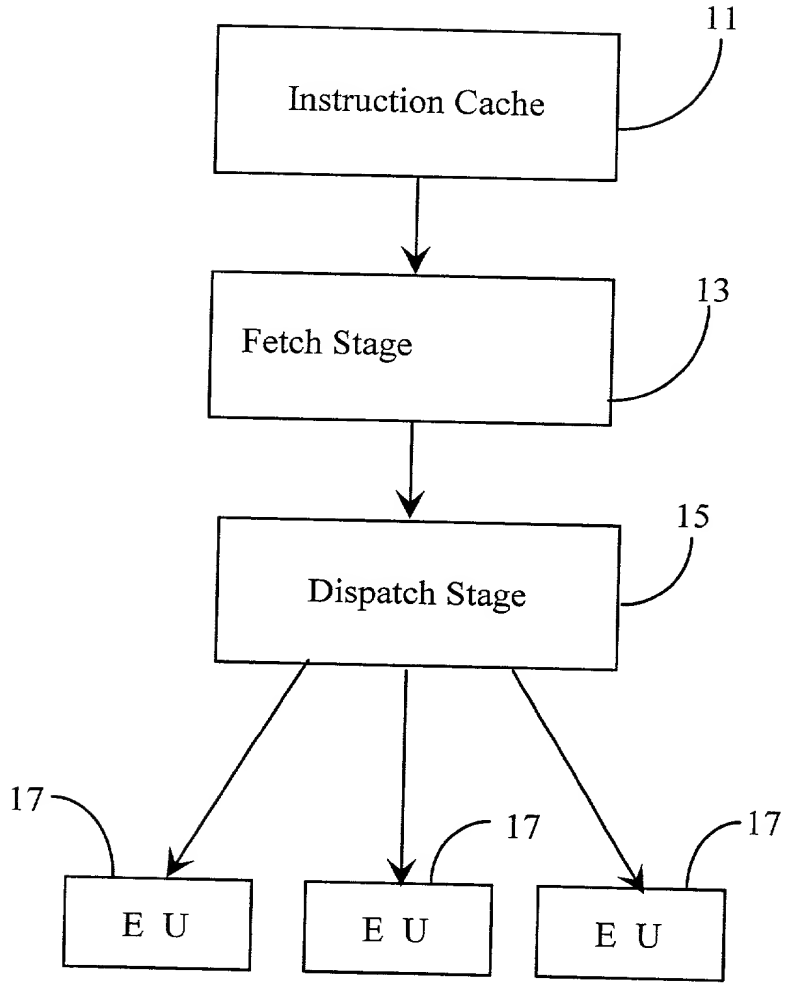

Fig. 1 (Prior Art)

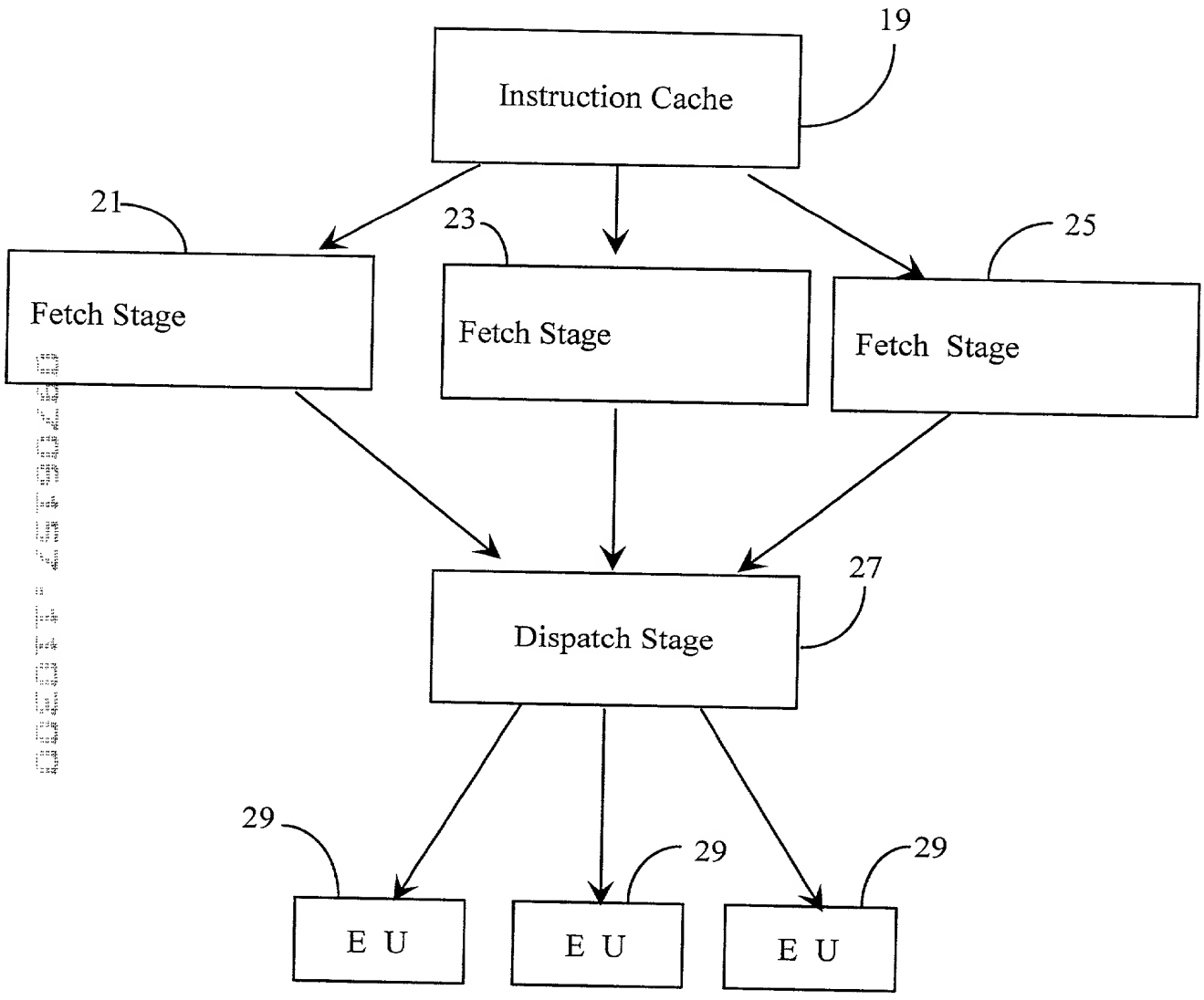
19
Instruction Cache
21
Fetch Stage
23
Fetch Stage
25
Fetch Stage
27
Dispatch Stage
29
E U
29
E U
29
E U

Fig. 2

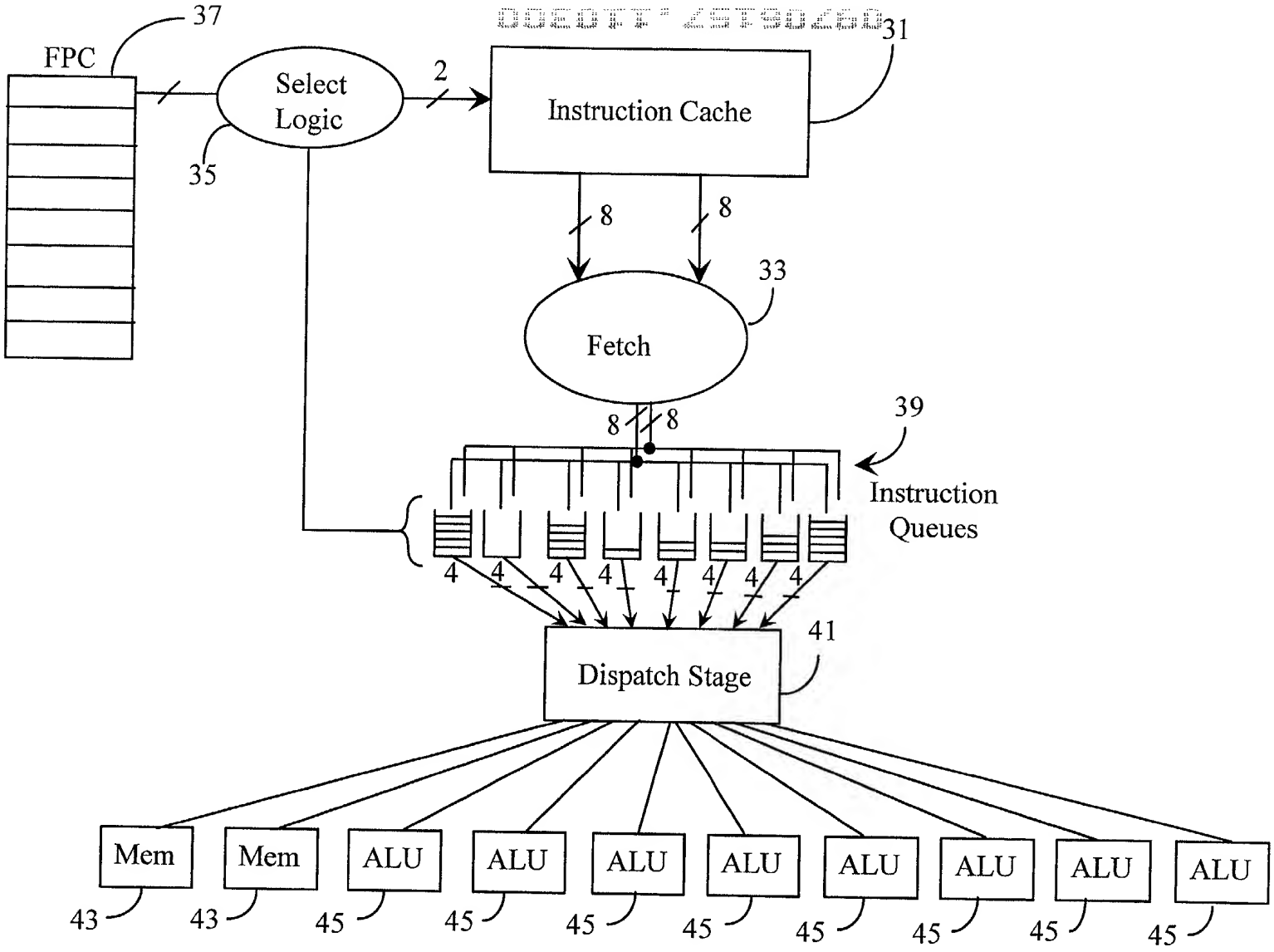
37
FPC
Select Logic
2
31
Instruction Cache
35
8
8
33
Fetch
8
8
39
Instruction Queues
4
4
4
4
4
4
4
4
41
Dispatch Stage
Mem
Mem
ALU
ALU
ALU
ALU
ALU
ALU
ALU
ALU
43
43
45
45
45
45
45
45
45
45

Fig. 3

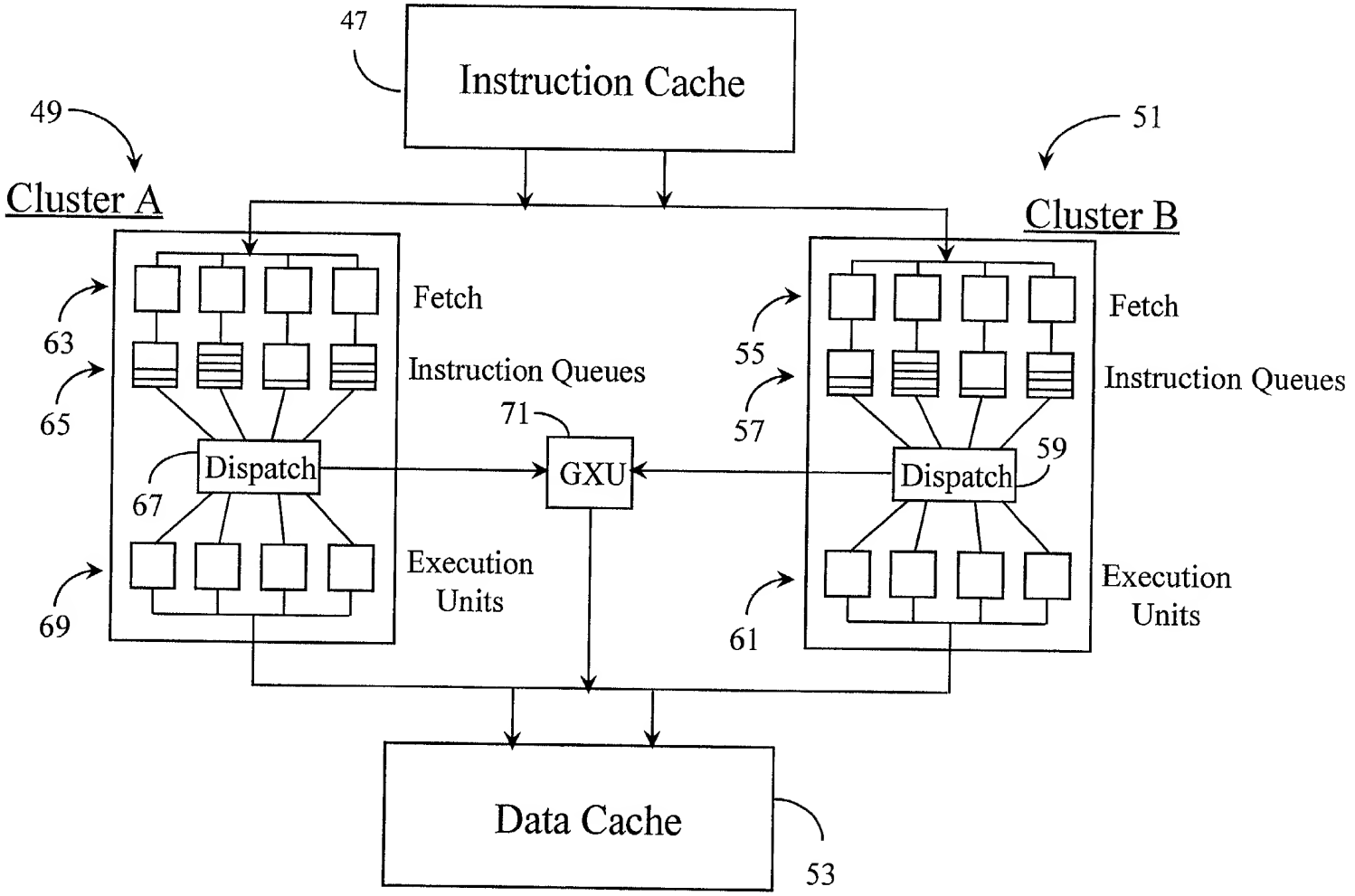
47
Instruction Cache
49
51
Cluster A
Cluster B
Fetch
Instruction Queues
63
65
55
57
71
Dispatch
GXU
Dispatch
59
67
Execution
Units
Execution
Units
69
61
Data Cache
53

Fig. 4

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

ATTORNEY DOCKET NO.3817

As a below named inventor, I hereby declare that: My residence, post office address and citizenship are as stated below next to my name. I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: **Clustering Stream and/or Instruction Queues for Multi-Streaming Processors**

the specification of which (check one) ☒ is attached hereto.
☐ was filed on:
☐ Application Serial No.
☐ and was amended on
(If applicable)

I hereby state that I have reviewed and understood the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, s 1.56 (a). In the case that the present application is a continuation-in-part application, I further acknowledge the duty to disclose material information as defined in 37 CFR s 1.56(a) which became available between the filing date of the prior application and the filing date of the present application. I hereby claim foreign priority benefits under Title 35, United States Code s119 of any foreign applications for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)

(Number) (Country) (Day/Month/Year Filed)

(Number) (Country) (Day/Month/Year Filed)

I hereby claim the benefit under Title 35, United States Code, s120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, s112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, s156(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

(Application Serial No.): _____ (Filing Date): _____ (Status): _____
(Application Serial No.): _____ (Filing Date): _____ (Status): _____
(Application Serial No.): _____ (Filing Date): _____ (Status): _____
(Application Serial No.): _____ (Filing Date): _____ (Status): _____
(Application Serial No.): _____ (Filing Date): _____ (Status): _____

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.
(List name and registration number)

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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6th inventor's signature: _____ Dated:
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Full name of 7th joint inventor, if any:

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Full name of 8th joint inventor, if any:

8th inventor's signature: _____ Dated:
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Post Office Address: